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METHOD TO PRODUCE TRANSISTOR HAVING REDUCED GATE HEIGHT

Abstract

Disclosed is a method and system of forming an integrated circuit transistor having a reduced gate height that forms a laminated structure having a substrate, a gate conductor above the substrate, and at least one sacrificial layer above the gate conductor. The process patterns the laminated structure into at least one gate stack extending from the substrate, forms spacers adjacent to the gate stack, dopes regions of the substrate not protected by the spacers to form source and drain regions adjacent the gate stack, and removes the spacers and the sacrificial layer.